AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 3, as follows:

This is a continuation of U.S. application Serial No. 10/144,748, entitled "Security System For Video Game System With Hard Disk Drive And Internet Access Capability", now U.S. Patent No. 6,712,704, which is a continuation of U.S. application Serial No. 09/384,189, now U.S. Patent No. 6,468,160, entitled "Security System For Video Game System With Hard Disk Drive And Internet Access Capability", which is a continuation-in-part of U.S. application Serial No. 09/288,293, now U.S. Patent No. 6,599,194, entitled "Home Video Game System With Hard Disk Drive and Internet Access Capability", which applications are hereby incorporated by reference herein in their entirety.

Please amend the paragraph beginning at page 3, line 1, as follows:

In ~~copending parent application Serial No. 09/288,293~~commonly assigned U.S. Patent No. 6,599194, a system is described which advantageously converts a heretofore stand alone, special purpose video game system into a network communicating device with bulk storage capacity having numerous enhanced capabilities such as simultaneous game play video and Internet display. As used herein, the "Internet" refers to the vast collection of interconnected networks that all use the TCP/IP protocols as well as the more generic interconnection of two or more networks.

Please amend the paragraph beginning at page 3, line 20, as follows:

With the addition of a modem and hard drive to a home video game system, the piracy issues become dramatically more serious and complex. For example, the personal computer industry has faced rampant end user piracy and the system described herein and in ~~copending application serial number 09/288,293~~ U.S. Patent No. 6,599,194 is likely to face the same type of pirating attacks.

Please amend the paragraph beginning at page 5, line 11, as follows:

In accordance with an exemplary embodiment of the present invention, each expansion device includes a unique ID associated with its mass media storage device. Unique encryption keys are advantageously used for each expansion device to ensure secure communications between the expansion device and the server. Thus, when a request is made through expansion device for downloading, for example, a particular video game, the server is able to rely on the request coming from an authorized expansion device and not an unauthorized device mimicking the expansion device.

Please amend the paragraph beginning at page 5, line 23, as follows:

In accordance with an exemplary embodiment of the present invention, the disk controller also incorporates an encrypting engine which encrypts in accordance with a highly secure encrypting algorithm.

Please amend the paragraph beginning at page 13, line 3, as follows:

In accordance with one exemplary implementation, to set up the video game system 50 for game play, the user first connects console 52 to color television set 58 by hooking a cable 78 between the two. Console 52 produces both "video" signals and "audio" signals for controlling color television set 58. The "video" signals control the images displayed on the television screen 60 and the "audio" signals are played back as sound through television loudspeaker 62. Depending on the type of color television set 58, it may be necessary to connect a conventional "RF modulator" between console 52 and color television set 58. This "RF modulator" (not shown) converts the direct video and audio outputs of console 52 into a broadcast type television signal (e.g., for a television channel 2 or 3) that can be received and processed using the television set's internal "tuner." Other conventional color television sets 58 have direct video and audio input jacks and therefore don't need this intermediary RF modulator.

Please amend the paragraph beginning at page 14, lines 12-13, as follows:

Controllers 56 may take a variety of forms and the controller depicted in Figure 1A is only for illustrative purposes only. In this example, the controllers 56a,b include various function controlling push buttons such as 84a-c and X-Y switches 86a,b used, for example, to specify the direction (up, down, left or right) that a player controllable character displayed on television screen 60 should move. Other controller possibilities include joysticks, mice pointer controls, a keyboard, and a wide range of other conventional user input devices. The presently preferred controller for use in system 50 is disclosed in Figures 6 through 7 of the applicants' assignee's copending application serial number 08/719,019, entitled "Operation Controlling Device and Video Processing System Used Therewith", now U.S. Patent 6,001,015, which ~~application~~ is incorporated herein by reference in its entirety.

Please amend the paragraph beginning at page 16, lines 4-5, as follows:

Video game console 52, as shown in Figures 1A, 1B, and 2, is coupled to game controllers 56. In accordance with one embodiment of the present invention, Internet operations may be controlled via a game controller 56 as shown in the above-identified ~~application Serial No. 08/719,019~~Patent 6,001,015. However, a preferred Internet access input device is a keyboard which permits convenient text entry operations. A wired keyboard may, for example, be coupled to one of the controller ports 80A-80D shown in Figure 1A and will preferably interface with the same control logic as a game controller 86. Alternatively, a wireless infrared keyboard or the like could be used as a text entry device.

Please amend the paragraph beginning at page 21, lines 17-18, as follows:

Prior to describing further details of expansion device 95, the video game system 50 will be described in conjunction with Figure 2, which is a block diagram of an illustrative embodiment of console 52 coupled to a game cartridge 54. Figure 2 shows a main processor 100, a coprocessor 200, and main memory 300 which may include an RDRAM expansion module 302. For a more complete description of the video game system shown in Figure 2, including details of the peripheral interface 138 and other components, reference is made to the applicants' assignee's copending application serial number 08/562,288, entitled "High Performance/Low Cost, Video Game System With

Multifunctional Peripheral Processing Subsystem", now U.S. Patent 6,022,274, which ~~application~~ is incorporated herein by reference in its entirety.

Main processor 100 is the computer that executes the video game program within storage device 54 in conjunction with coprocessor 200. In this example, the main processor 100 accesses this video game program through the coprocessor 200 over a communication path 102 between the main processor and the coprocessor 200, and over another communication path 104_a,b between the coprocessor and the video game storage device 54. Alternatively, the main processor 100 can control the coprocessor 200 to copy the video game program from the video game storage device 54 into main memory 300 over path 106, and the main processor 100 can then access the video game program in main memory 300 via coprocessor 200 and paths 102, 106. Main processor 100 accepts inputs from game controllers 56 during the execution of the video game program.

Please amend the paragraph beginning at page 23, line 6, as follow

Figure 2 also shows that the audio video outputs of coprocessor 200 are not provided directly to television set 58 in this example, but are instead further processed by external electronics outside of the coprocessor. In particular, in this example, coprocessor 200 outputs its audio and video information in digital form, but conventional home color television sets 58 require analog audio and video signals. Therefore, the digital outputs of coprocessor 200 must be converted into analog form -- a function performed for the audio information by DAC and mixer amp 40 and for the video information by VDAC and encoder 144. The analog audio signals generated in DAC 140 are amplified and filtered by an audio amplifier therein that may also mix audio signals generated externally of console 52 via the EXTSOUND L/R signal from connector 154. The analog video signals generated in VDAC 144 are provided to a video encoder therein which may, for example, convert ~~8~~RGB~~s~~ inputs to composite video outputs compatible

with commercial TV sets. The amplified stereo audio output of the amplifier in ADAC and mixer amp 140 and the composite video output of video DAC and encoder 144 are provided to directly control home color television set 58. The composite synchronization signal generated by the video digital to analog converter in component 144 is coupled to its video encoder and to external connector 154 for use, for example, by an optional light pen or photogun.

Please amend the paragraph beginning at page 24, lines 1-14, as follows:

In this illustrative embodiment, game controllers 56 are not connected directly to main processor 100, but instead are connected to console 52 through serial peripheral interface 138. Serial peripheral interface 138 demultiplexes serial data signals incoming from up to four or five game controllers 56 (e.g., 4 controllers from serial I/O bus 151 and 1 controller from connector 154) and provides this data in a predetermined format to main processor 100 via coprocessor 200. Serial peripheral interface 138 is bidirectional, i.e., it is capable of transmitting serial information specified by main processor 100 out of front panel connectors 80a-d in addition to receiving serial information from those front panel connectors. The serial interface 138 receives main memory RDRAM data, clock signals, commands and sends data/responses via a coprocessor serial interface (not shown). I/O commands are transmitted to the serial interface 138 for execution by its internal processor as is described in U.S. Patent 6,022,274~~copending application Serial No. 08/562,288~~. In this fashion, the peripheral interface, ~~its processor~~ by handling I/O tasks, reduces the processing burden on main processor 100. As is described in more detail in U.S. Patent 6,022,274~~application Serial No. 08/562,288~~, serial peripheral

interface 138 also includes a "boot ROM (read only memory)" that stores a small amount of initial program load (IPL) code. This IPL code stored within the peripheral interface boot ROM is executed by main processor 100 at time of startup and/or reset to allow the main processor to begin executing game program instructions 108 within storage device 54. The initial game program instructions 108 may, in turn, control main processor 100 to initialize the drivers and controllers it needs to access main memory 300.

Please amend the paragraph beginning at page 27, line 16, as follows:

Storage device 54 also stores coprocessor microcode 156. In this example, a signal processor within coprocessor 200 executes a computer program in order to perform its various graphics and audio functions. This computer program, called the "microcode," is provided by storage device 54. Typically, main processor 100 copies the microcode 156 into main memory 300 at the time of system startup, and then controls the signal processor to copy parts of the microcode on an as-needed basis into an instruction memory within signal processor for execution. Because the microcode 156 is provided by storage device 54, different storage devices can provide different microcodes -- thereby tailoring the particular functions provided by coprocessor 200 under software control. Because the microcode 156 is typically too large to fit into the signal processor's internal instruction memory all at once, different microcode pages or portions may need to be loaded from main memory 300 into the signal processor's instruction memory as needed. For example, one part of the microcode 156 may be loaded into signal processor 400 for graphics processing, and another part of microcode may be loaded for audio processing.

Please amend the paragraph beginning at page 64, line 19, as follows:

The preferred alternative security system (as shown in Figure 11) also utilizes communication between security processor 180 and a security processor resident in video game system 50 as is further disclosed in U.S. Patent Application Serial No. 08/850,676, entitled "SYSTEMS AND METHODS FOR PROVIDING SECURITY IN A VIDEO GAME SYSTEM", now U.S. Patent 6,071,191, which is herein incorporated by reference. As described in detail in the copending application, when a player wants to a play a particular video game and is using an external storage containing the desired video game, a security microprocessor embodied within the external storage is coupled to the video game system 50. Upon power up, the security microprocessor within the external storage, e.g., game cartridge, sends an authentication key and an authentication code to a security processor resident within the peripheral interface 138 shown herein in Figure 2. The peripheral interface 138 sends the authentication key to the video game main processor. The peripheral interface 138 retains the authentication code and does not reveal it to the video game system 50 main processor. The peripheral interface 138 of the main game unit has a copy of the same computation program used at the manufacturing facility.

Please amend the paragraph beginning at page 65, lines 13-14, as follows:

The peripheral interface 138 includes a boot ROM that stores this computation program. The computation program is executed in the video game system 50 in a security processor resident within the external game cartridge. Assuming the external cartridge is authentic the main processor of the video game system 50 and the processor in the game cartridge, generate the same computation result, or one that bears a predetermined relationship with the result obtained by the counterpart processor. If the results are different, the game processor will not be permitted to execute the video game programs in the cartridge. A similar methodology is utilized in accordance with one embodiment of the present invention using the security processor 180 and boot ROM 182 of the expansion dev ice 95. Other security features described ~~in the assignee's copending Application Serial No. 850,676~~ U.S. Patent 6,071,191 are preferably utilized in conjunction with security processor 180.

Please amend the paragraph beginning at page 71, line 14, as follows:

For(i = 1_*to*_n), $H_i = E_{Mi}(H_{i-1})$-⊕ ⊗H_{i-1} that is graphically shown in Figure 14,

Please amend the paragraph beginning at page 72, lines 1-2, as follows:

$M_{1\_to\_n}$ are 128 bit blocks of **clear text blocks** of the text to be hashed.

⊗⊕-is a 128 bit wide bitwise XOR operation,